REMARKS

Claims 21-23 and 43 are pending in the present application. Claim 43 has been amended.

Claim Rejections-35 U.S.C. 112

Claim 43 has been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. This rejection is respectfully traversed for the following reasons.

Although Applicant does not necessarily agree that the term "substantially" in claim 43 renders the claim indefinite to one of ordinary skill, claim 43 has been amended to feature that "the wiring delay times of said third and fourth signal paths are set to be substantially equal by setting a length of said first wiring that connects said fourth pad with said output terminal of said first selector to be substantially the same as a length of said second wiring that connects said third pad with said output terminal of said second selector". Thus, the first and second wirings are set to be substantially the same, so that the wiring delay times of the third and fourth signal paths are substantially equal. Applicant respectfully submits that one of ordinary skill would readily understand the scope of claim 43. Applicant therefore respectfully submits that claim 43 is in compliance with 35 U.S.C. 112, second paragraph, and thus respectfully urges the Examiner to withdraw this rejection.

Claim Rejections-35 U.S.C. 103

Claims 21-23 and 43 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kurihara reference (Japanese Patent Publication No. 2000-030492) in view of the Lee et al. reference (U.S. Patent No. 5,661,685) and the Ozaki reference (U.S. Patent No. 5,337,321). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 21 includes in combination a fourth signal path which has provided therein a first wiring and a first selector, and a third signal path which has provided therein a second wiring and a second selector. An output terminal of the first selector is connected with the fourth pad by the first wiring, and an output terminal of the second selector is connected with the third pad by the second wiring. The first selector outputs a prescribed signal, or a test clock which is input to the clock input terminal of a circuit block. In addition, the third and fourth signal paths are formed so that wiring delay time of the third and fourth signal paths are substantially equal.

In view of these features, the semiconductor device of claim 21 can measure access time exactly, as described in the Amendment dated February 26, 2004. In other words, the access time of the circuit block is measured exactly only by: subtracting [the time from when a test clock is input to the second pad until the test clock is output from the fourth pad], from [the time from when a test input signal is input to the first pad until a test output signal is output from the third pad].

For performing exact measurements, the wiring delay time of the third and fourth

signal paths are featured in claim 21 as substantially equal. Therefore, as described on page 7, lines 18-19 of the present application with respect to Fig. 1, multiplexer 105 is disposed in the vicinity of multiplexer 104, and only wiring is used for connecting multiplexers 104 and 105 respectively to pads 109 and 110. Particularly, in the case where multiplexers 104 and 105 are disposed in vicinity of each other, and only wiring is used for connecting multiplexers 104 and 105 with pads 109 and 110, delay time of the corresponding signal paths from macro cell 101 to pads 109 and 110 can be substantially equal.

In contrast, the Kurihara reference discloses a technology for measuring the access time of memory circuit 1 by using flip-flop circuit 2, selection circuitry 3 and delay circuit 4. That is, the circuit in Fig. 1 of the Kurihara reference includes a signal path for guiding a data output D0 to an output pad through flip-flop circuit 2, and a signal path for guiding a test clock to an output pad through selection circuitry 3 and delay circuit 4.

However, the Kurihara reference does not disclose that delay time of these signal paths are set to be equal. The Examiner has asserted that wiring delay times of these signal paths in memory circuit 1 that provide respective outputs TD0 and TCK become substantially equal, when the delay of flip-flop circuit 2 is controlled to be the same as the amount of delay in delay circuit 4. However, the Kurihara reference does not teach that the delay of flip-flop circuit 2 is controlled to be the same as the amount of delay in delay circuit 4. **That is, as described in paragraph [0021] of the English**

translation of the Kurihara reference, the delay time of delay circuit 4 is adjusted so that phase difference between clock signal CLK input to memory circuit 1 and holding clock signal TCK input to flip-flop circuit 2 become minimum within the range where flip-flop circuit 2 can hold the output signal D0 from memory circuit 1. As further described in paragraph [0027] of the English translation of the Kurihara reference, the value of this minimum phase difference depends on the access time of memory circuit 1. Therefore, the delay time of the signal path for outputting the signal TD0 and the delay time of the signal path for outputting the signal TCK, are not substantially equal in the Fig. 1 circuit of the Kurihara reference.

The Ozaki reference as relied on by the Examiner discloses a circuit comprising flip-flop 22 wherein selectors 25, 28 and 26 are respectively connected to a data input terminal D, a clock terminal C and an output terminal Q of flip-flop 22. However, the Ozaki reference does not specifically describe a circuit which comprises a signal path for guiding an output signal from terminal Q of flip-flop 22 to an output pad, that has substantially equal wiring delay time as a signal path for guiding a clock from terminal C of flip-flop 22 to an output pad. The Ozaki reference therefore does not teach that access time can be measured exactly by setting delay time of corresponding signal paths substantially equal.

The Lee et al. reference as relied upon by the Examiner discloses a semiconductor device provided with a probe pad, but does not disclose corresponding signal paths to the third and fourth pads as in claim 21. The Lee et al. reference thus

does not teach that access time of a circuit block can be measured exactly by setting delay time of corresponding signal paths substantially equal.

Applicant therefore respectfully submits that the semiconductor device of claim 21, including in combination a circuit block; first through fourth signal paths; first and second selectors; and first and second wirings, wherein the third and fourth signal paths are formed so that wiring delay time of the third and fourth signal paths are substantially equal, would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together. Applicant therefore respectfully submits that this rejection of claims 21-23 and 43 is improper for at least these reasons.

Conclusion

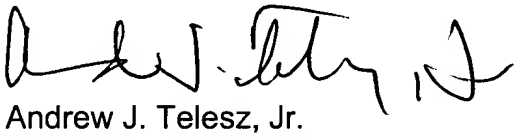
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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